

A 1-8 GHz, 190MHz BB BW Mixer-First Receiver With Bootstrapped Mixer Switches Achieving Over 16dBm In-Band IIP₃

Erwin Hardeveld¹, Graduate Student Member, IEEE, Ronan van der Zee¹, Member, IEEE, and Bram Nauta¹, Fellow, IEEE

Abstract—In this article, we propose a wideband mixer-first receiver with improved in-band (IB) linearity. It uses bootstrapped N-path mixer switches to achieve a constant ON-state gate-source voltage for large IB signals. We analyze the tradeoff between ON-state resistance and OFF-state subthreshold current in conventional mixer switches and introduce a method to break this tradeoff with the presented bootstrap technique. The mixer is followed by a degenerated LNTA featuring partial cancellation of its nonlinear output current. The receiver is fabricated in 22-nm FDSOI CMOS and achieves over 16-dBm IB IIP₃ at room temperature and over 14-dBm IIP₃ over the industrial temperature range. It has a 190-MHz I and Q baseband bandwidth, while its performance is demonstrated for a local oscillator frequency range from 1 to 8 GHz.

Index Terms—Bootstrapping, high linearity, in-band (IB) linearity, LNTA, mixer first, N-path, receiver, wideband.

I. INTRODUCTION

IN-BAND linearity is becoming increasingly important in wideband receiver design. The introduction of carrier aggregation and higher order modulation schemes increasingly challenges the receiver's linearity and blocker compression point, especially when in-band (IB) blockers are present.

Most receivers that aim to address the growing bandwidth and linearity requirements can be divided into two groups, namely, passive mixer-first receivers and LNTA-first receivers. Passive mixer-first receivers [1], [2], [3], [4], [5] are known for their good linearity, as the passive mixer can be highly linear. Amplification is done in baseband, where the signal frequencies are much lower and feedback can be used to linearize the amplifiers. LNTA-first receivers [6], [7], [8] offer isolation between antenna and receiver and generally have lower noise but have lower linearity than passive mixer-first receivers. Optimizing the LNTA for very high linearity is challenging since the LNTA needs to cover the entire RF

Received 12 February 2025; revised 23 May 2025 and 18 July 2025; accepted 31 August 2025. This article was approved by Associate Editor Hongtao Xu. This work was supported in part by the Research Program “ZERO: Toward Energy Autonomous Systems for IoT” through the Dutch Research Council (NWO) under Grant P15-06. (Corresponding author: Erwin Hardeveld.)

The authors are with the Integrated Circuit Design Group, University of Twente, 7522 NB Enschede, The Netherlands (e-mail: e.hardeveld@utwente.nl).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JSSC.2025.3606117>.

Digital Object Identifier 10.1109/JSSC.2025.3606117

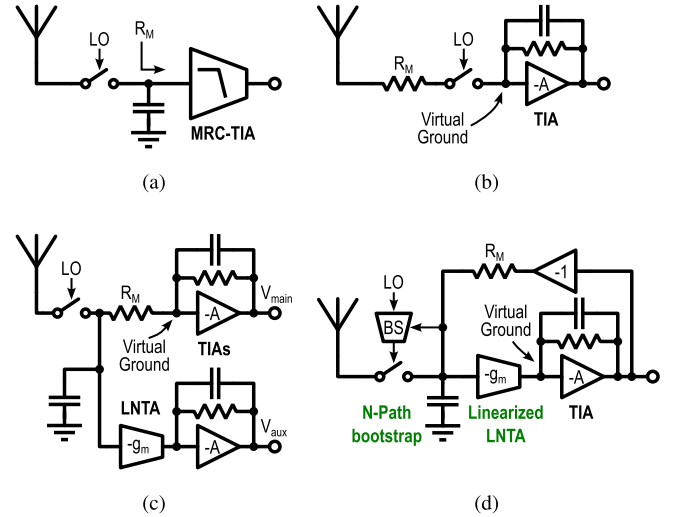


Fig. 1. Overview of passive mixer-first receiver architectures (one path shown). (a) Wideband receiver with MRC-based TIA [1]. (b) Receiver with a passive matching resistor and TIA with virtual ground [2]. (c) Wideband receiver with baseband noise cancellation [3]. (d) Proposed receiver with bootstrapped switches.

range, which is large in software-defined radio architectures. Our goal is high linearity; therefore, this work is based on a passive mixer-first topology.

In [1], a passive mixer-first receiver is published that has a wide bandwidth and good selectivity. A system overview is shown in Fig. 1(a). The high selectivity is achieved through a “modified regulated cascode” (MRC) amplifier, which achieves 40 dB/dec selectivity at the baseband node. However, the low IB IIP₃ of −12 dBm makes it susceptible to distortion when large IB signals are present. This can be attributed to the high IB voltage swing at the mixer switches and at the input of the baseband amplifier.

The receiver shown in Fig. 1(b) [2] uses a resistor for RF V–I conversion and matching, a passive mixer, and a baseband TIA for I–V conversion. Since the resistor is passive and the mixer sees the TIA’s virtual ground, linearity is excellent. The linearity of the TIA is enhanced through a negative conductance parallel to the opamp’s virtual ground canceling distortion currents. A downside of this topology is that the 50 Ω RF resistor increases the minimum achievable NF by 3 dB, resulting in poor noise performance. A similar

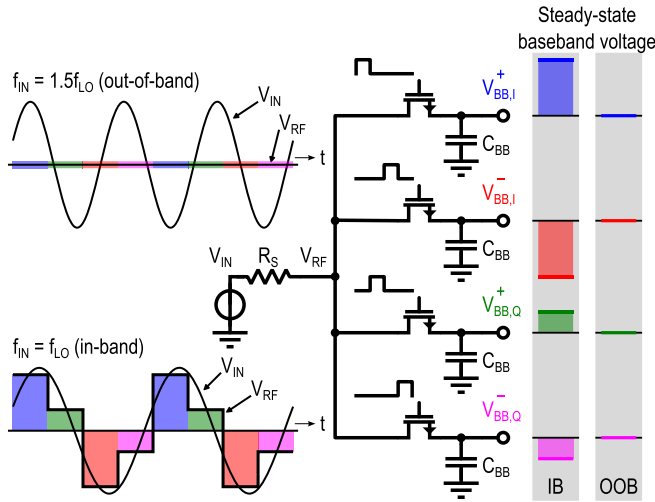


Fig. 2. N-path filter with four paths assuming $R_S \cdot C_{BB} \gg T_{on}$. The RF and baseband signals can be seen at the left and right sides of the figure, respectively. An OOB signal with $f_{in} = 1.5f_{LO}$ results in no baseband signal swing, an IB signal with $f_{in} = f_{LO}$ has a large-signal swing.

receiver for mmW frequencies is presented in [9]. In addition to feedback linearization, the matching resistor R_M is added separately to each mixer path so that overlapping clocks can be used. This reduces the effect of rise/fall time on the mixer's linearity.

To alleviate the noise penalty of the matching resistor R_M , a baseband noise-canceling architecture is presented in [3], as shown in Fig. 1(c). An auxiliary path is added after the mixer, consisting of an LNTA and a TIA, canceling the noise of the main path. Since the LNTA is in baseband, it can be linearized using degeneration without compromising the RF frequency range. However, this comes with a major increase in power consumption and, similar to the receiver in Fig. 1(a), linearity is limited by the baseband voltage swing at the switches.

In this work, we propose the receiver in Fig. 1(d). It features a bootstrap circuit specifically designed for N-path mixer switches, followed by an LNTA that partially cancels its nonlinear output current. The receiver is designed to operate over a broad range of RF input frequencies with high IB linearity and bandwidth, demonstrating that these techniques can be applied in a variety of (software-defined) radios. In Sections II and III, we analyze the IB linearity of the mixer switches and the LNTA and propose circuits to improve their IB linearity. Section IV provides the receiver's schematic level design, and Section V presents the measurement results.

II. BOOTSTRAPPED N-PATH FILTER

This work features a bootstrapped passive mixer that improves the IB linearity of N-path filters. A basic N-path filter is shown in Fig. 2 [10], consisting of four mixer switches driven by four-phase nonoverlapping clocks with frequency f_{LO} . The input signal V_{IN} with frequency f_{IN} is filtered and mixed to baseband, resulting in the signal V_{BB} with frequency $f_{IN} - f_{LO}$.

For out-of-band (OOB) signals, the linearity of N-path passive mixers has proven to be excellent [4]. This is because

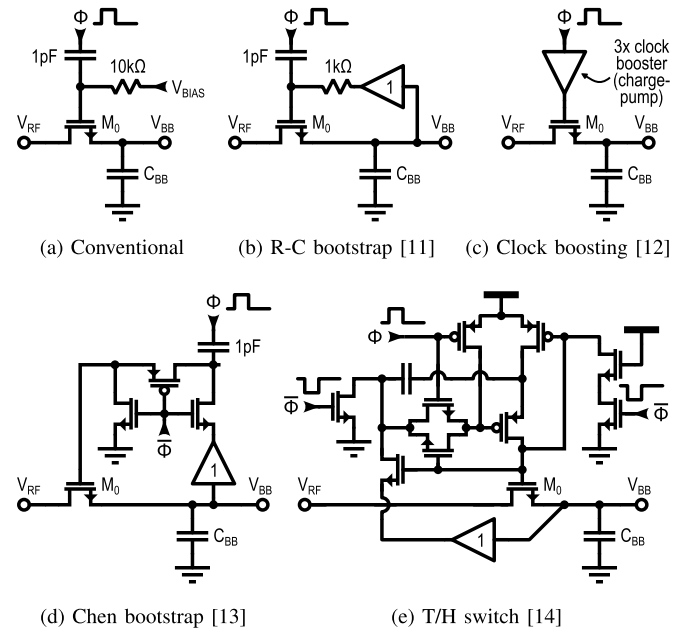


Fig. 3. Prior art switch drivers for N-path filters. (a) Conventional N-path switch with a static bias voltage applied to the gate. V_{BIAS} is optimized for linearity. (b) RC bootstrap based on [11], with an RC frequency of 160 MHz. (c) Clock boosting circuit based on [12] with $V_{G,off} \approx V_{DD}$ and $V_{G,on} \approx 2V_{DD}$. (d) Bootstrap circuit based on [13], with an additional switch isolating the buffer in the ON-state [15]. (e) T/H switch [14], where V_{BB} is connected through an ideal buffer.

OOB signals are filtered, resulting in reduced signal swing at nodes V_{RF} and V_{BB} , as illustrated in the top left of Fig. 2. Therefore, the mixer switch sees only minor voltage variations at its drain and source and thus has good linearity.

In contrast to OOB signals, IB signals are not filtered, which means that the mixer switches see the full signal swing at their source and drain, as indicated at the bottom of Fig. 2. This gives rise to two nonlinear effects. First, in the ON-state, the switch resistance R_{on} is modulated due to variations in the gate-source voltage. Second, in the OFF-state, there is signal-dependent non-zero subthreshold current due to gate-source and gate-drain voltage variations. Both effects will be analyzed and improved by the clock bootstrapping technique presented in the remainder of this section.

A. Prior Art

Fig. 3(a) shows a conventional circuit used to drive N-path mixer switches. A bias voltage V_{BIAS} is applied to the gate, which can be tuned to optimize linearity. Prior art has proposed different techniques to improve the linearity of passive mixers. In [11], the baseband voltage is superimposed on the gate as a bias voltage through the use of an RC circuit, as shown in Fig. 3(b). For low baseband frequencies, this results in a constant overdrive voltage when the switch is on, reducing R_{on} modulation. For signal frequencies near the -3 dB bandwidth of this RC network, the phase of the superimposed signal shifts, degrading the effectiveness of this method. Unfortunately, this RC frequency cannot be increased indefinitely, as it affects the clock swing negatively because the clock is high-pass-filtered by the same network.

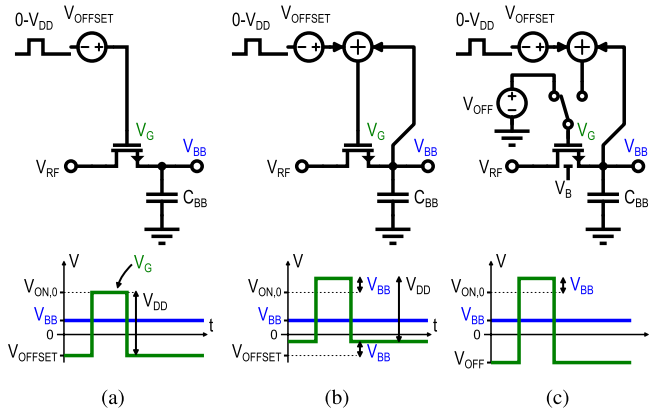


Fig. 4. N-path circuit (one path drawn) with three different clock driving circuits. $V_{on,0}$ is the ON-state gate voltage if $V_{BB} = 0$. (a) Conventional driver. (b) Baseband voltage added to gate voltage. (c) Baseband voltage added and $V_G = V_{off} = -0.4$ V in OFF-state.

In [12], an N-path filter is proposed that uses clock boosting to achieve high linearity and a high gain compression point, as shown in Fig. 3(c). Using a charge pump, the clock signal swing is boosted to $3V_{DD}$ such that the gate voltage is $2V_{DD}$ in the ON-state and $-V_{DD}$ in the OFF-state. In this way, the OFF-state current and ON-state resistance are both reduced. The disadvantages of this method are that the clock power increases significantly and that the gate-source voltage of the switch exceeds V_{DD} , which requires the use of thick-oxide devices to avoid reliability issues.

In [13], the baseband voltage of an N-path filter is added to the clock signal using two additional switches and a capacitor, as shown in Fig 3(d). Compared to [11], the bandwidth limitation is alleviated, but the additional switches see drain-source and gate-source voltages larger than V_{DD} , raising reliability concerns.

A circuit that is often used in track and hold (T/H) applications is the bootstrap switch [16], as shown in Fig. 3(e). This circuit is designed such that the gate follows the source voltage in the ON-state, while the gate is reset to ground in the OFF-state, greatly reducing R_{on} modulation. T/H bootstrap switches are often used in applications with a sub-GHz clock frequency; as we will see, high-frequency operation is an issue.

B. Switch Nonlinearity in N-Path Filters

In order to better understand the IB IIP₃ of N-path filters and the tradeoff between ON-resistance and subthreshold current, we performed transient simulations with three different idealized gate driving circuits, as shown in Fig. 4. The mixer switch is a minimum length SLVT NMOS in 22 nm FDSOI technology with $R_{ON} \approx 6.5 \Omega$ (when $V_{GS} = V_{DD} = 0.8$ V) and V_T around 250 mV. The N-path filter consists of four paths with a baseband bandwidth of 200 MHz ($C_{BB} = 6$ pF) and is driven from a 50 Ω source. A baseband shunt matching resistor (not shown) is used to provide matching to the RF source. The clock frequency f_{LO} is 4 GHz.

The non-overlapping clocks are generated by ideal sources and are buffered with two inverters using a V_{DD} supply voltage. V_{OFFSET} is added to the clock signal after the clock buffers with

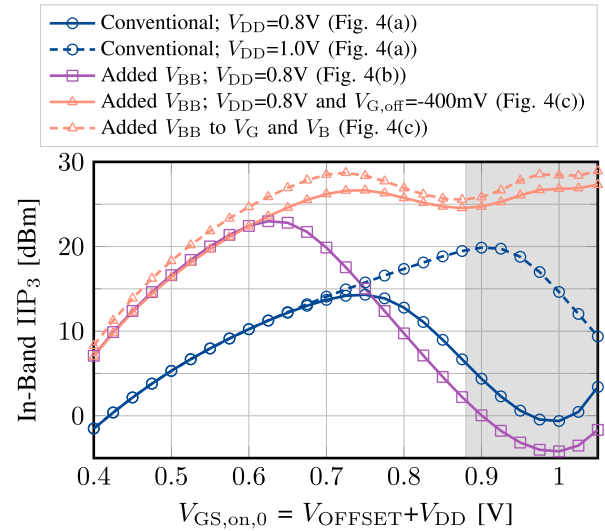


Fig. 5. Simulated N-path IB linearity for the clock techniques shown in Fig. 4. V_{OFFSET} is varied and $V_{GS,on,0}$ is the ON-state gate-source voltage when $V_{BB} = 0$. Gate-source voltages exceeding the technology voltage limitations are made gray.

an ideal voltage source. The switch used in Fig. 4(c) is ideal and enabled when the clock is lower than 50 mV.

The simulated IIP₃ is shown in Fig. 5 ($f_1 = f_{LO} + 48$ MHz, $f_2 = f_{LO} + 52$ MHz, and $f_{IM3} = 44$ MHz). We performed simulations for different values of V_{OFFSET} ($V_{GS,on,0} = V_{OFFSET} + V_{DD}$ is shown on the x-axis, where $V_{GS,on,0}$ is the gate-source voltage when $V_{BB} = 0$ V).

The circuit in Fig. 4(a) directly drives the mixer switch with V_{DD} swing and offset V_{OFFSET} . An increased V_{OFFSET} (larger $V_{GS,on}$) decreases R_{on} modulation thanks to the increased overdrive. The sub-threshold current contribution in the OFF-state increases with increasing V_{OFFSET} , as $V_{GS,off}$ increases. In Fig. 5, we see that this results in an optimum IIP₃ of 14 dBm at $V_{GS,on,0} = 750$ mV ($V_{DD} = 0.8$ V), corresponding to $V_{GS,off} = V_{OFFSET} = -50$ mV. Linearity can be improved by increasing V_{DD} , as both R_{on} and the OFF-state current are reduced. Simulations with $V_{DD} = 1.0$ V (for insight, this exceeds the technologies voltage limitation) show an optimum at $V_{GS,on} = 900$ mV, with a 5.5 dB better IIP₃.

The circuit shown in Fig. 4(b) adds the baseband voltage to the clock signal. This reduces R_{on} modulation, as $V_{GS,on}$ becomes independent of V_{BB} . However, in the OFF-state, $V_{GD,off}$ becomes larger when V_{BB} is positive. Because the MOSFET is symmetric, drain and source can be interchanged, and the increased $V_{GD,off}$ leads to an increased reverse OFF-state current. The IB IIP₃ simulation in Fig. 5 confirms this; the optimum is found at $V_{GS,on} = 625$ mV and is 8.6 dB higher than the previous circuit with $V_{DD} = 0.8$ V. However, IIP₃ quickly degrades for higher values of $V_{GS,on}$.

The last circuit, shown in Fig. 4(c), adds the baseband voltage to the clock signal in the ON-state and sets the gate voltage to V_{off} in the OFF-state. This method benefits from reduced R_{on} modulation, while the OFF-state current is minimized with a constant OFF-state gate voltage V_{off} , breaking the tradeoff (there is no way to make $V_{GD,off}$ and $V_{GS,off}$ signal-independent at the same time to completely eliminate signal-dependent

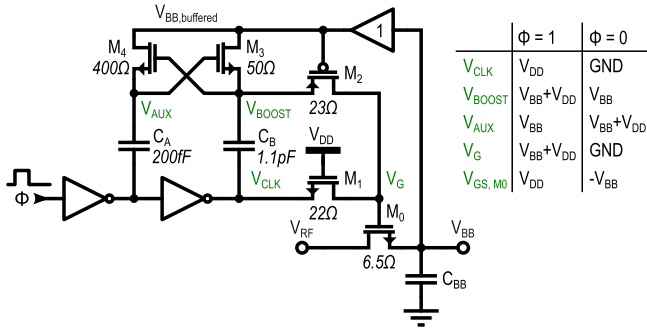


Fig. 6. Schematic of the proposed N-path switch with bootstrapping.

OFF-state current). Linearity simulations with $V_{off} = -400$ mV show an IB IIP₃ of > 26 dBm and no degradation for higher $V_{GS, on}$. When V_{BB} is added to both V_G and the backgate V_B of the switch to reduce the body effect, the linearity increases slightly with another 1 to 2 dB.

C. Bootstrap Implementation

We can conclude that the highest IB IIP₃ can be achieved with a circuit that has a signal-independent V_{GS} in the ON-state and a negative V_{GS} in the OFF-state. However, it is difficult to design a switch that achieves these two requisites and still has the fast rise and fall time required to operate up to 8 GHz f_{LO} . Therefore, two simplifications are made to design a highly linear bootstrapped switch.

First, in an N-path filter, the baseband voltage V_{BB} does not change significantly over a clock period since $f_{LO} \gg f_{-3dB, BB}$. To obtain a signal-independent V_{GS} , while the switch is on, we can use a sampled value of the source voltage (V_{BB}) as it is approximately constant during a clock period. Following from this, V_{BB} is available when the switch is off, making it possible to store this voltage on a bootstrap capacitor when the switch is off, for use when the switch turns on.

Second, when a positive dc bias voltage is applied to the baseband capacitors, a negative V_{GS} is obtained in the OFF-state by pulling the gate to ground. This dc bias voltage is also beneficial for the subsequent baseband amplifiers since it makes ac coupling redundant.

A circuit schematic implementing bootstrapping with these two simplifications is shown in Fig. 6. The buffered clock V_{CLK} is directly connected to the bottom plate of the bootstrap capacitor C_B . Transistor M_2 turns on when the clock is high and connects the top plate of C_B to the gate of M_0 , charging it to $V_{BB} + V_{DD}$.

When the clock is low, M_1 discharges the gate of M_0 to ground, while M_3 charges the bootstrap capacitor C_B to the baseband voltage V_{BB} . In order to turn on M_3 , an auxiliary path consisting of C_A and M_4 is added to boost the gate of M_3 to $V_{BB} + V_{DD}$ similar to the Nakagome charge pump [17]. The on-resistance of M_3 is approximately 50Ω so that the voltage on C_B settles within a few f_{LO} cycles.

This bootstrap circuit generates a constant $V_{GS, M0} = V_{DD}$ in the ON-state and a negative $V_{GS, M0}$ in the OFF-state, assuming that $f_{LO} \gg f_{-3dB, BB}$. Under this assumption, the $V_{GS, M0}$

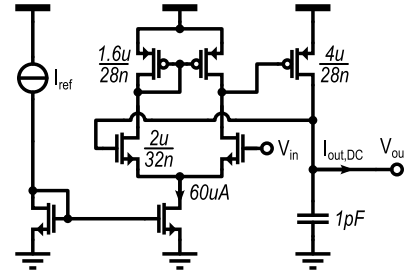
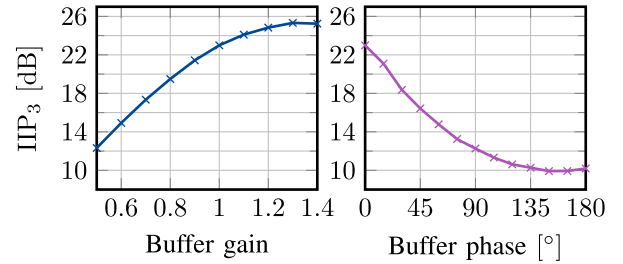


Fig. 7. Schematic of the buffer between the baseband node and the bootstrap circuit.

Fig. 8. Simulated IB IIP₃ at $\Delta f = 50$ MHz of the bootstrapped N-path front end with different gains and phase shifts in the buffer. $f_{LO} = 4$ GHz.

waveform is similar to that of a T/H switch [16], but our circuit is much simpler. The number of intermediate nodes is kept to a minimum to ensure correct operation up to $f_{LO} = 8$ GHz with fast rise and fall time. All drain–source and gate–source voltages remain within the technology’s limitations to ensure reliability.

D. Bootstrap Buffer

As the baseband node is biased at a dc voltage, there is a dc voltage on the bootstrap capacitor C_B . During every clock cycle, some charge is transferred from C_B to the gate of M_0 , which needs to be replenished in the charging phase. This results in a dc current flow from the baseband node V_{BB} to the bootstrap switch that is dependent on the clock frequency. We placed a buffer between the baseband node and the bootstrap switch to eliminate this dc current from the baseband node, relaxing the receiver’s common-mode feedback circuit (otherwise, this buffer is not required, as the small-signal input impedance of the bootstrap circuit is much larger than the required matching impedance at baseband). Fig. 7 shows the schematic of the buffer. The common-source output stage is biased with the dc current ($I_{out, DC}$) drawn by the bootstrap switch (more on this later).

We simulated the effect of gain error and phase shifts in the buffer on the bootstrap switch’s IIP₃. Fig. 8 shows the result. Linearity is highest with a gain larger than one. We expect that this is the result of charge sharing between the bootstrap capacitor C_B and the parasitic capacitance at node V_{BOOST} (see Fig. 6). The IIP₃ only varies with approximately 2.5 dB for buffer gains between 0.9 and 1.1. Phase shifts in the buffer have a much larger effect. A phase shift of 45° degrades the IIP₃ with more than 6 dB. Therefore, we designed a buffer that has a closed-loop bandwidth of more than 1 GHz, limiting the phase error at 200 MHz to approximately 10° .

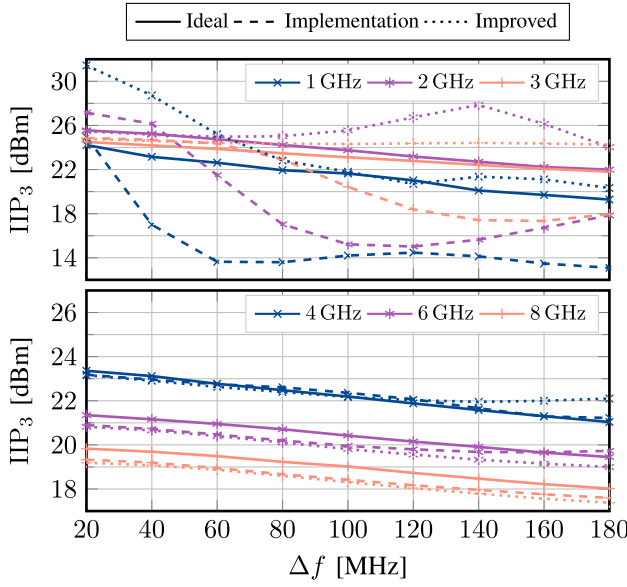


Fig. 9. Simulated IIP₃ of the bootstrapped N-path frontend with ideal and transistor implemented bootstrap buffer (Fig. 7). Simulations with an improved buffer design are added with a dotted line.

E. Simulation

We simulated the transistor implementation of the bootstrap switch over a range of f_{LO} with both an ideal buffer and the buffer from Fig. 7. The resulting IIP₃ is shown in Fig. 9 ($f_1 = f_{LO} + \Delta f - 2$ MHz, $f_2 = f_{LO} + \Delta f + 2$ MHz, and $f_{IM3} = \Delta f - 6$ MHz). For $f_{LO} = 4$ GHz and larger, the ideal and transistor implemented buffer perform similarly. For f_{LO} smaller than 4 GHz, the IIP₃ of the front end with transistor implemented buffer is severely degraded. This is due to a decrease in the output current $I_{out,DC}$, which is linearly dependent on f_{LO} (approximately 25 μ A/GHz). This limits both g_m (bandwidth) and the slewing rate of the buffer's output stage, introducing gain and phase errors. Unfortunately, this was only discovered during measurement but can easily be improved with an additional 65 μ A current source connected to the output node, increasing the bias current of the common-source stage. This adds approximately 0.2 mW power consumption to the receiver. The simulated IIP₃ of the front end with improved buffer is added to Fig. 9 with dotted lines.

The simulation results for $f_{LO} = 1$ GHz show a slightly lower IIP₃ than the result for $f_{LO} = 2$ GHz. We expect this to be the case as f_{-3dB} is approaching f_{LO} . The IIP₃ degrades slightly for $f_{LO} = 6$ GHz and $f_{LO} = 8$ GHz. We hypothesize that this is due to an increasing contribution of the clock transitions since these become more relevant compared to the decreasing on-time.

F. Comparison With Prior Art

The IB IIP₃ of the proposed N-path filter switch (Fig. 6) has been simulated together with the prior art discussed in Section II-A (Fig. 3). All circuits drive a mixer switch (M_0) that has the same dimensions as the switch used in Section II-B. The other transistors and LO buffers are scaled for a fast rise and fall time until no significant improvement

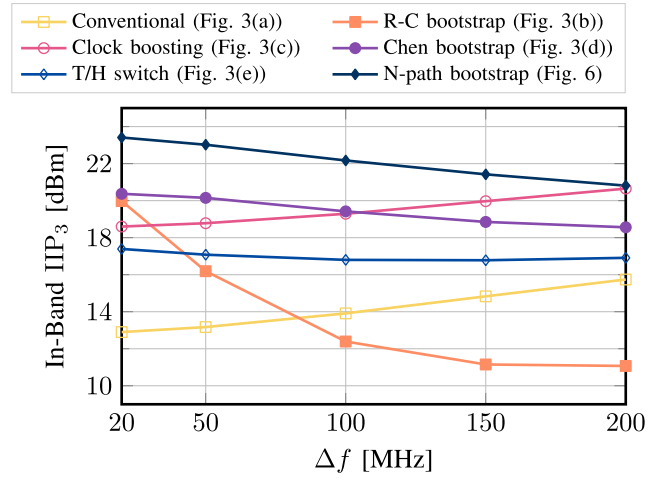


Fig. 10. Simulated N-path IB linearity for different schematics level implementations at $f_{LO} = 4$ GHz.

TABLE I

SIMULATED N-PATH P_{1dB} , RISE/FALL TIME, NF, AND I_{DC} FOR DIFFERENT SWITCH DRIVER DESIGNS ($f_{LO} = 4$ GHz)

Design	P_{1dB} [dBm]	t_r/t_f [ps]	NF [dB]	I_{DC} [μ A]	I_{Buf} [μ A]
Conventional (Fig. 3(a))	-1.0	5.7/5.3	1.5	432	-
R-C bootstrap (Fig. 3(b))	-0.9	5.3/5.1	1.7	532	-
Clock boosting (Fig. 3(c))	6.1	12.8/13.6	1.8	1783	-
Chen bootstrap (Fig. 3(d))	3.2	7.6/20.7	1.8	747	63
T/H switch (Fig. 3(e))	6.4	14.2/15.2	1.9	825	430
This Work (Fig. 6)	6.9	9.0/7.8	1.5	730	99

is seen. The buffer between V_{BB} and the rest of the circuits is modeled as ideal to isolate BB loading effects and to eliminate the nonlinear effects of the actual buffer. The four-phase nonoverlapping clocks are generated using a transistor-level Windmill clock divider [18] (Section IV-A).

The mixer switches are embedded in an N-path front end with four paths and 200 MHz baseband bandwidth ($C_{BB} = 6$ pF). V_{BB} and V_{RF} are biased at $V_{DD}/2$. A noiseless baseband shunt matching resistor (not shown) is used to provide matching to the 50 Ω RF source.

The IB IIP₃ for $f_{LO} = 4$ GHz is shown in Fig. 10. Two input tones are applied to the RF input at $f_1 = f_{LO} + \Delta f - 2$ MHz and $f_2 = f_{LO} + \Delta f + 2$ MHz. The resulting baseband IM₃ tone is at $\Delta f - 6$ MHz. Additionally, Table I shows the 1 dB gain compression point, gate rise and fall time, NF at 50 MHz, and the supply current of the simulated designs. The gain compression point is simulated using an input signal at $f_{LO} + 50$ MHz.

I_{dc} is the average current consumption of one mixer switch with its driving circuit, including two inverter LO buffers. I_{Buf} is the average current supplied from the buffer connected between the baseband node and the switch drivers.

The conventional switch design [Fig. 3(a)] achieves approximately 13 dBm IB IIP₃. Linearity is 3 dB better at the -3 dB bandwidth due to signal attenuation. The conventional design has the fastest rise and fall time and the lowest power consumption among the tested designs.

The RC-based bootstrapped switch [11] [Fig. 3(b)] has 20 dBm IIP₃ at low offset frequencies, but this degrades quickly for larger offset frequencies due to attenuation and phase shift introduced by the clock RC network. At offset frequencies over 80 MHz, the IIP₃ is even worse than that of the conventional switch.

The switch with boosted clock [12] [Fig. 3(c)] achieves 18.6 dBm IIP₃, which increases by 2 dB at the band edge. The rise and fall times of this switch are long due to the large voltage swing on the gate, but the slew rate at the gate is slightly higher than the conventional switch. The power consumption is the highest among the tested designs.

The bootstrap switch proposed in [13] [Fig. 3(d)] has a IIP₃ between 20.4 and 18.6 dBm. Rise time is similar to the conventional switch when swing is taken into account, but it has a long fall time due to a gate delay used to generate the inverted clock.

This bootstrap design [13] [Fig. 3(d)] and the $3 \cdot V_{DD}$ clock boosting design [12] [Fig. 3(c)] were implemented using core devices, although not all gate–source or drain–source voltages are within the technology limits. Therefore, these designs cannot be reliably fabricated with core devices, and thick-oxide devices should be used instead, causing degradation of performance.

The T/H switch [14] [Fig. 3(e)] achieves a 17.4 dBm IIP₃, which degrades to 16.9 dBm toward the band edge. However, the rise and fall times are slow due to the large number of intermediate nodes between the clock input and the gate of the mixer switch M_0 . In addition, a large current I_{Buf} is drawn from the output of the buffer isolating the baseband node.

Our newly proposed bootstrap circuit (Fig. 6) provides the highest IB IIP₃ of 23.4–20.8 dBm. This is achieved by keeping the ON-state gate–source voltage of the mixer switch independent of V_{BB} while ensuring good isolation in the OFF-state by having a negative gate–source voltage. We also minimized the number of internal nodes, resulting in a rise and fall time similar to the conventional switch when a $1.5V_{DD}$ V_G swing on the gate is considered. This makes it possible to use the switch at high clock frequencies and reduces the nonlinearity produced during clock transitions.

Its 1 dB compression point is also improved, allowing it to handle large RF signal swings. The power consumption is the lowest compared to the switches with wideband improved IIP₃ and blocker compression point. The noise figure (NF) is similar to that of conventional N-path mixers. All gate–source and drain–source voltages remain within the technology limitations such that the circuit can be reliably implemented.

III. DEGENERATED LNTA WITH PARTIAL DISTORTION CANCELLATION

Since the IB linearity of the passive mixer is significantly improved through bootstrapping, an LNTA with an equally high linearity is desired to achieve good overall IB receiver linearity.

A. Linearization Principle

Inverter-based LNTAs are known for their good power-per-noise performance due to the inherent bias current re-use.

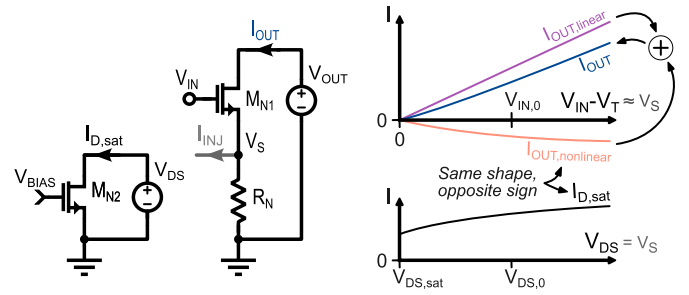


Fig. 11. Nonlinear current in a degenerated inverter (1) and the current of a transistor on the edge of saturation $I_{D,sat}$, which is similar in shape but opposite in sign. Adding $I_{D,sat}$ to I_{OUT} (by injecting it at I_{INJ}) yields a linearized output current. Currents are not to scale; only the NMOS side is shown.

The linearity of an inverter can be optimized by appropriately scaling the NMOS and PMOS, but the result is highly PVT sensitive [19], [20].

A more robust method to linearize an inverter is to add degeneration. Increasing the degeneration resistance increases IIP₃ at the cost of bandwidth and voltage headroom [3], but it also reduces the overall transconductance and introduces noise. In our work, the main limiting factor is the voltage supply of 0.8 V, which is not enough to achieve the linearity that we want with degeneration alone.

In [20], analysis shows that the dominant source of third-order distortion in a degenerated inverter is the transistor's second-order distortion. A “floating battery” is introduced between the sources of the NMOS and PMOS to short-circuit the second-order current, improving IIP₃. Although this concept works at RF using a capacitor, in our case, it would be challenging to achieve a low impedance over a wide baseband bandwidth as this requires a large capacitance.

In this work, we take another approach. We add bleeding transistors parallel to the degeneration resistors of a degenerated LNTA, partly canceling the nonlinear current at the output of the LNTA. To explain the concept, Fig. 11 shows the N-side of a degenerated inverter LNTA (M_{N1} and R_N). The dominant source of distortion in a transistor is second order; therefore, we model the MOSFET according to the square law model (where $\beta_N = \mu_N C_{OX}(W/L)$). The output current is

$$I_{OUT} = \underbrace{\frac{V_{IN} - V_T}{R_N}}_{I_{OUT,linear}} + \underbrace{\frac{1 - \sqrt{1 + 2\beta_N R_N (V_{IN} - V_T)}}{\beta_N R_N^2}}_{I_{OUT,nonlinear}}. \quad (1)$$

Two parts can be distinguished: a linear part and a nonlinear part containing a square root. Both contributions are plotted at the top right of Fig. 11. We also plotted the drain current $I_{D,sat}$ of the MOSFET M_{N2} just in saturation as a function of V_{DS} at the bottom right of Fig. 11. We make two observations. First, the nonlinear component of the output current $I_{OUT,nonlinear}$ has a similar but opposite shape compared to the drain current $I_{D,sat}$ of a MOSFET in saturation. Second, the voltage V_S in Fig. 11 equals $I_{OUT} \cdot R_N$, which is proportional to V_{IN} (ignoring the nonlinear output current). Also, when a current I_{INJ} is injected at this node, it adds up to the output current I_{OUT} when $g_{m,N1} R_N \gg 1$.

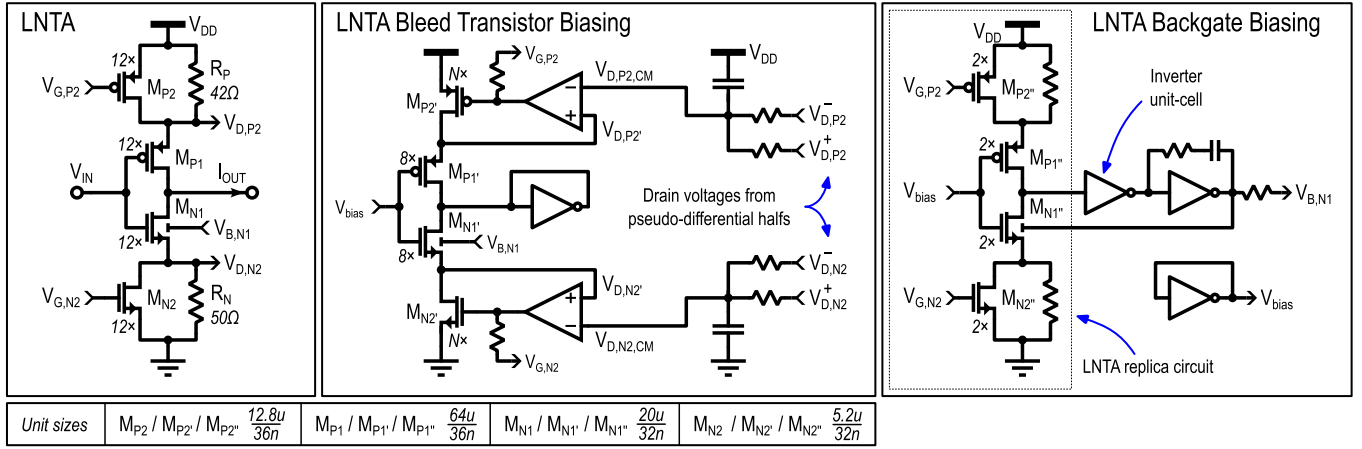


Fig. 12. Schematic of the proposed LNTA including biasing circuits.

Therefore, when we connect the drain of MOSFET M_{N2} to V_S with appropriate biasing (V_{BIAS} and $V_{DS,0}$) and width, we can partially cancel the nonlinear current of the degenerated transistor M_{N1} at the output I_{OUT} without additional power consumption (excluding the biasing circuit). We do not have analytical expressions for the nonlinearity cancellation because simplified transistor models (e.g., square law model) do not accurately describe the nonlinear behavior of the transistor at the edge of saturation, but Sections III-B and III-C provide simulation results showing large-signal performance and robustness to PVT spread.

B. LNTA Implementation

The schematic of our self-biased LNTA with nonlinearity cancellation is shown on the left side of Fig. 12. The bias voltages $V_{G,N2}$ and $V_{G,P2}$ control the amount of current through the bleed transistors M_{N2} and M_{P2} . The backgate voltage $V_{B,N1}$ controls the zero-current output voltage of the LNTA. The total transconductance of the LNTA is 33.4 mS.

The current through the bleed transistors M_{N2} and M_{P2} is a ratio of the total bias current through M_{N1} and M_{P1} . This ratio is derived in a replica bias circuit, shown in the middle of Fig. 12, and can be programmed with a transistor ratio N . The bleed biasing circuit consists of eight parallel replica transconductors ($M_{N1'}$ and $M_{P1'}$) with N bleed transistors ($M_{N2'}$ and $M_{P2'}$) and no degeneration resistors. The gate voltages $V_{G,N2}$ and $V_{G,P2}$ of the bleed transistors are set so that the drain voltage of the replica bleed transistors is equal to the common-mode drain voltage in the actual LNTA. In this condition, the current density in the replica transconductors $M_{N1'}$ and $M_{P1'}$ is the same as that in the actual LNTA such that the current through the bleed transistors M_{N2} and M_{P2} is $(8/N)$ times the current through M_{N1} and M_{P1} . N can be programmed from 20 to 40.

The zero-current output voltage of the LNTA is set with the backgate of M_{N1} . This bias voltage is generated using a scaled-down LNTA replica circuit, shown on the right side of Fig. 12. A unit-cell inverter with the same dimensions as used in the OPAMP (described in Section IV-B) measures the output voltage, and another inverter drives the backgate of M_{N1} .

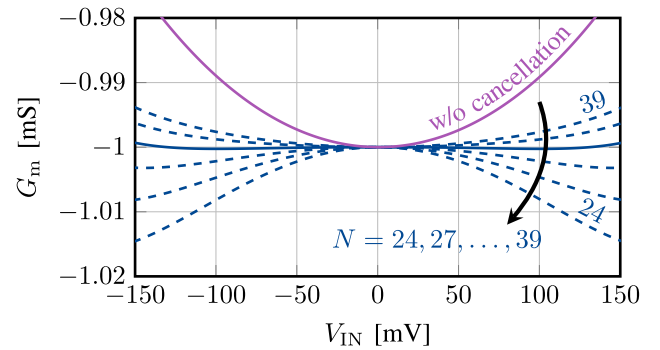


Fig. 13. Normalized large-signal transconductance G_m of the pseudo-differential LNTA with and without nonlinearity cancellation for different values of N . V_{IN} is relative to the input bias point. $N = 33$ gives the best linearity.

so that the replica's output voltage matches the self-bias point of the op-amp.

To ensure stability between the feedback loops for the backgate voltage $V_{B,N1}$ and the bleed transistors, the bandwidth of the loops setting the bleed bias is much smaller than that of the loop setting the backgate voltage. Also, in the bleed biasing loops, the gain from $V_{G,N2'}$ to $V_{D,N2'}$ is much larger than the positive feedback from $V_{G,N2}$ to $V_{D,N2,CM}$ so that the differential input voltage ($V_{D,N2'} - V_{D,N2,CM}$) of the biasing amplifier always sees negative feedback.

The simulated large-signal transconductance G_m of the pseudo-differential LNTA is shown in Fig. 13 for different values of N to illustrate the distortion cancellation. For increasing N , the bleed current is reduced so that the amount of nonlinear current with opposite shape added to the output of the LNTA is reduced. Optimal nonlinearity cancellation is observed for $N = 33$. The bleeding transistors add approximately 10% to the LNTA's output noise, as the current through the bleeding transistors is limited and other noise contributions are dominating.

C. Robustness Over PVT

The LNTA linearization relies on the cancellation of two effects that are roughly opposite in shape but not physically correlated. This raises PVT robustness concerns. Since their

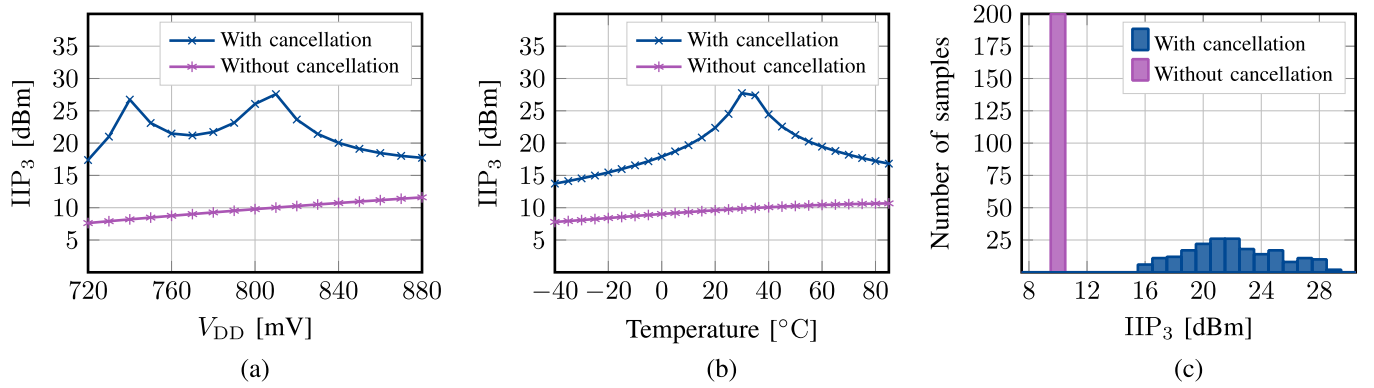


Fig. 14. Simulations of the IIP₃ of the degenerated LNTA with and without partial nonlinearity cancellation over: (a) V_{DD} voltage variation, (b) temperature, and (c) only mismatch spread (Monte Carlo with 200 samples). The simulations have been performed with two input tones at 98 and 102 MHz.

shape is opposite, an improvement in linearity is expected, even if there is a mismatch in shape. To quantify this improvement, IIP₃ simulations are performed that incorporate PVT variations. The biasing circuit is included in these simulations. The bleed ratio N is fixed to 33 for all simulations, unless otherwise indicated.

Fig. 14(a) shows the IIP₃ of the LNTAs for a supply voltage variation of $\pm 10\%$. The LNTA with cancellation achieves an IIP₃ which is at least 6 dB higher than that of the degenerated LNTA. Fig. 14(b) shows the IIP₃ over a temperature ranging from -40 °C to 85 °C, showing an improvement of at least 6 dB.

A Monte Carlo simulation with 200 samples is performed to show the linearity improvement over mismatch variations. The result is shown in Fig. 14(c). The IIP₃ of the LNTA with cancellation has more spread than the degenerated LNTA, but the lowest IIP₃ out of 200 samples is still 6 dB higher.

Similar mismatch simulations were done for different process corners (SS, FF, SF, and FS) at -40 °C, 25 °C, and 85 °C, each with 200 samples. In these simulations, the optimal value of N was programmed for each corner and temperature through a “batch calibration.” The improvement in linearity compared to the degenerated LNTA over all these simulations is at least 5 dB. In the case where no process corner and temperature calibration is performed and N is fixed to 33, the improvement is still at least 2 dB, while most samples perform much better.

Hence, this linearization technique can give us a noticeable increase in IIP₃ compared to a regular degenerated LNTA, at no additional power cost (excluding biasing).

IV. RECEIVER DESIGN AND SIMULATION

Fig. 15 shows the full receiver, driven from a single-ended $50\ \Omega$ RF source. The detailed schematics of the bootstrap Switch, Bootstrap buffer, and the LNTA are found in Figs. 6, 7, and 12. The receiver is designed to operate over an LO range of 1–8 GHz but is optimized for $f_{LO} = 4$ GHz.

A. N-Path Front End and Clock Generation

The N-path front end consists of four mixer switches with minimum length and $R_{ON} \approx 6.5\ \Omega$. The value of C_{BB} is $5.4\ \text{pF}$, which, together with the input capacitance of the LNTA,

gives an N-path filter baseband bandwidth of approximately 200 MHz. The gates of the mixer switches are driven by the bootstrap circuit as introduced in Fig. 6 in Section II-C.

The clock signal is derived from an externally applied clock signal with frequency $2 \cdot f_{LO}$. The clock signal is first amplified with inverters and converted to a square wave, after which it is divided into a four-phase clock with 25% duty cycle. The clock divider is based on the Windmill divider [18], which provides a compact design with good phase noise performance. Its schematic is shown at the right of Fig. 15.

The simulated phase noise at the output of the clock divider and at the gates of the N-path switches (including the bootstrap driver) is shown in Fig. 16. The clock buffer before the divider is not included in the simulations. The phase noise of the divider is approximately $-167\ \text{dBc/Hz}$, while the phase noise at the gate of the N-path switches is approximately 2 dB higher.

B. TIA

We implemented the TIA using an OPAMP with a feedback network consisting of resistor R_F and capacitor C_F . R_F determines the transimpedance of the TIA and is $150\ \Omega$. C_F limits the bandwidth of the TIA to 350 MHz and is $3\ \text{pF}$.

In order to achieve the desired linearity, a three-stage inverter-based OPAMP is used for its high open-loop gain over a wide bandwidth [3]. The design is shown at the bottom right of Fig. 15. It is built from parallel inverter unit-cells with $12.7\ \text{mS}$ transconductance. The first inverter g_{m1} in the main path is scaled for noise, while the third inverter g_{m3} is scaled to drive the load. A Miller compensation network, consisting of C_C and R_C , sets the dominant pole. The feedforward inverter g_{m4} ensures 20 dB/dec roll-off at the unity-gain frequency.

Fig. 17 shows the simulated open-loop gain and phase response of the OPAMP, incorporating the load capacitance. The unity-gain bandwidth is 4.5 GHz and the open-loop gain at 200 MHz is 41 dB thanks to the second-order roll-off above 0 dB. The phase margin is 60° . Each OPAMP has approximately 4.6 mA bias current, of which half is spent in the fast-path g_{m4} to achieve the high unity-gain bandwidth.

Fig. 18 shows the resulting IIP₃ of the TIA. We simulated it together with an ideal $33.4\ \text{mS}$ transconductor modeling the

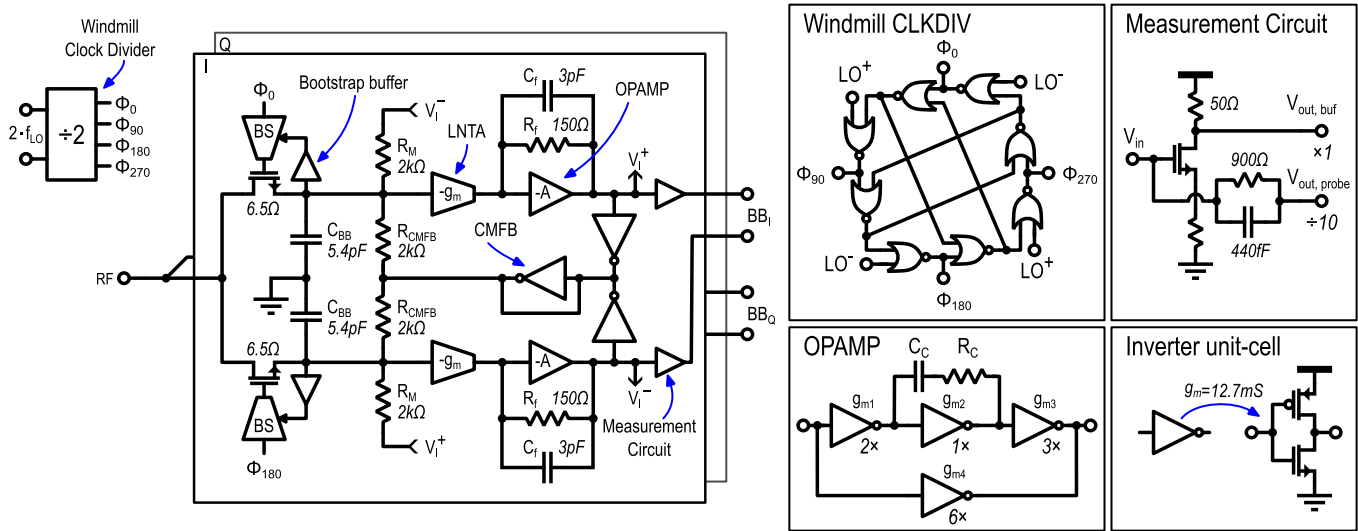


Fig. 15. Full system schematic of the bootstrapped N-path receiver, including the schematics of the clock divider, OPAMP, and measurement circuit. The OPAMP is based on the design in [3]. The non-overlapping clocks are generated using a clock divider based on the work in [18].

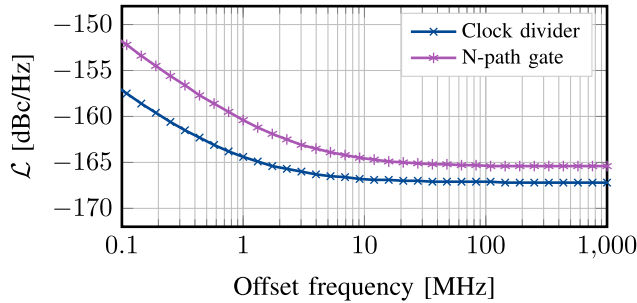


Fig. 16. Simulated phase noise at the output of the clock divider and at the gate of the N-path switch at $f_{LO} = 4$ GHz.

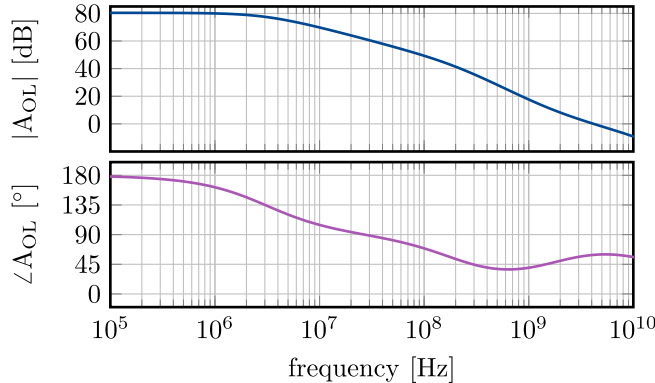


Fig. 17. Simulated open-loop gain and phase response of the OPAMP.

LNTA and a baseband model of the N-path filter. The IIP₃ is referred back to the RF input of the receiver, assuming that the N-path filter has no losses. The IIP₃ is more than 20 dBm at low offset frequencies. At higher frequencies the IIP₃ decreases due to the reduced open-loop gain of the OPAMP. Linearity increases around 180 MHz thanks to N-path filtering.

C. Matching and Common-Mode Feedback

The resistors R_M are used to achieve matching to a 50 Ω source impedance. They are placed around the baseband

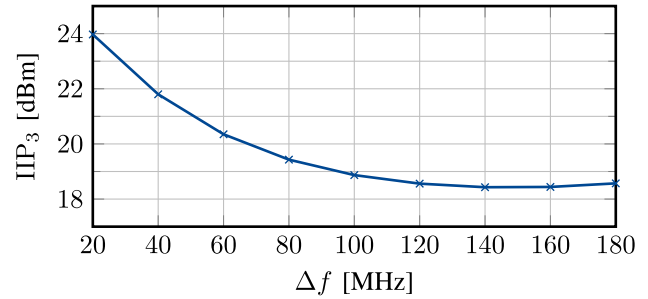


Fig. 18. Simulated IIP₃ of the TIA including a linear model of the N-path filter and LNTA.

amplifier to reduce their noise contribution and have a value of 2 k Ω . As the baseband amplifiers have a positive gain, the matching resistors are cross-coupled between the differential outputs to ensure negative feedback. However, this creates positive common-mode feedback. Therefore, we designed a common-mode feedback network that has a larger gain than the matching network to avoid instability.

The desired common-mode voltage at the output is the self-bias point of the inverters used in the OPAMP. Two inverter unit-cells convert the output voltages V_{I+} and V_{I-} into a current (see the top left of Fig. 15). These currents are added and converted to a voltage by a shunted inverter, yielding two times the CM voltage error. Two resistors R_{CMFB} apply the amplified CM error to the baseband nodes. The value of R_{CMFB} is the same as R_M such that the CMFB is stronger than the positive feedback from the matching network, even when the output is clipped to the supply. Choosing a larger R_{CMFB} would benefit noise performance, but makes it impossible for the circuit to recover from large CM disturbances.

D. Simulation Results

We simulated the receiver with and without the bootstrapped N-path switches and linearized LNTA to assess their linearity benefit. The simulation results are shown in Fig. 19 ($f_1 = f_{LO} + \Delta f - 2$ MHz, $f_2 = f_{LO} + \Delta f + 2$ MHz, and

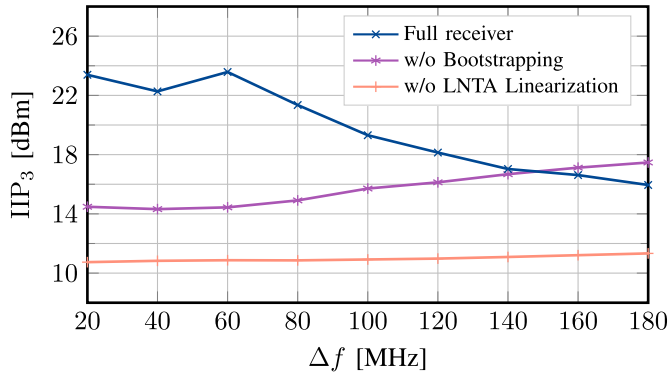


Fig. 19. Simulated IB IIP₃ at $f_{LO} = 4$ GHz with and without bootstrapped N-path switches and LNTA linearization.

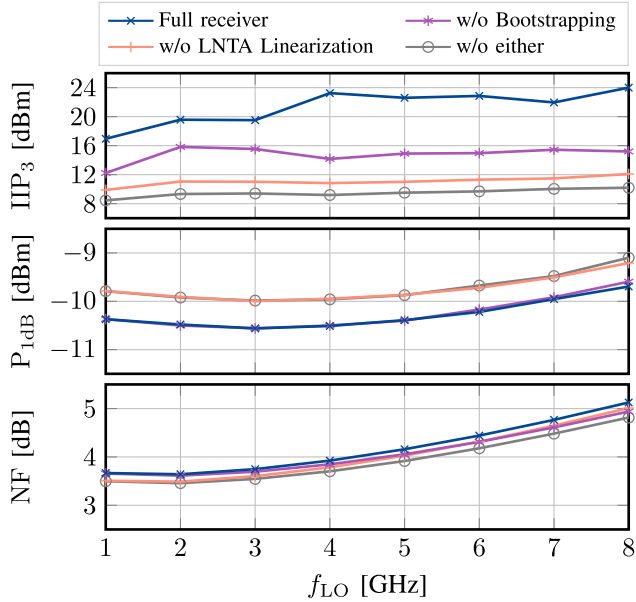


Fig. 20. Simulated receiver IB IIP₃, P_{1dB} , and NF with and without bootstrapped N-path switches and LNTA linearization. $\Delta f = 50$ MHz for all simulations.

$f_{IM3} = \Delta f - 6$ MHz). The full receiver has an IB IIP₃ of 23 dBm at low offset frequencies, corresponding to the front-end simulations in Section II-F. At higher offset frequencies, the IIP₃ decreases, as it is limited by the TIA (see Fig. 18).

When conventional N-path switches are used in the receiver, the IIP₃ drops to 14 – 17 dBm. This is similar to the results obtained in Section II-F. Above 150 MHz, the IIP₃ is slightly higher, expectedly due to cancellation of different IM₃ products. Disabling distortion cancellation in the LNTA reduces the IIP₃ of the receiver to approximately 11 dBm. Additionally, Fig. 20 shows the IB IIP₃, P_{1dB} , and NF for different LO frequencies at $\Delta f = 50$ MHz.

V. EXPERIMENTAL RESULTS

The receiver is fabricated in the 22 nm FDSOI CMOS process from GlobalFoundries and packaged in a 6×6 mm² QFN package. A die micrograph is shown in Fig. 21(a). The active area is 0.30 mm².

The chip is powered from a 0.8 V supply voltage and consumes 37.6 mW + 1.1 mW/GHz. A power breakdown at $f_{LO} = 4$ GHz is shown in Fig. 21(b). The contributions

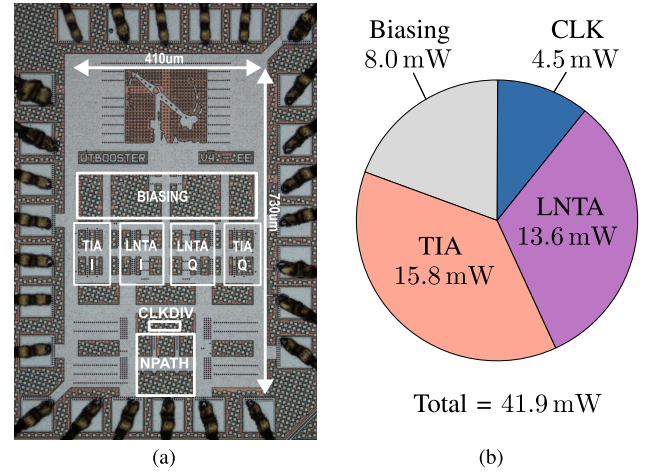


Fig. 21. Fabricated chip in 22 nm FDSOI CMOS and its power breakdown at $f_{LO} = 4$ GHz. (a) Chip micrograph. (b) Power breakdown.

of the LNTA, TIA, and biasing circuits are split from the total baseband power consumption based on their relative contributions extracted from simulation. The biasing circuitry has a relatively high power consumption, mainly for generating the bleed transistor bias, as it is optimized for programmability and not for low power. Its power consumption could be reduced by reducing the width of the replica circuit used for biasing the bleed transistors (at the cost of a larger step size of the bleed bias control) or by sharing the biasing circuitry between I and Q. For different f_{LO} , only the clock power contribution changes.

A. Measurement Setup

Two measurement circuits are implemented on-chip, as shown in the top right of Fig. 15. A buffer with 50 Ω output impedance and $1\times$ gain is implemented for noise and gain measurements. This buffer is combined with a 2:1 balun on the measurement PCB. The dc gain of the buffer is de-embedded from the measurement results through simulation. The baluns on PCB are de-embedded through measurement.

For the large-signal linearity measurements, a passive probe half-circuit is implemented on-chip. This circuit is terminated with a 4:1 balun for differential to single-ended conversion and the 50 Ω input impedance of the measurement equipment such that each half-circuit effectively sees 100 Ω and some parasitic capacitance. There is some mismatch in the probe circuit, but this is not an issue as the pole/zero pair lies outside the measurement bandwidth.

The current through the bleed transistors in the LNTA is set to approximately 31% of the LNTA bias current. This corresponds to a code of $N = 26$ and is used for all measurements and samples, including measurements at different ambient temperatures. Simulations are performed with $N = 33$. These values of N are chosen for optimal linearity at ambient temperature in measurement and simulation.

B. Measurement Results

The receiver's gain and $|S_{11}|$ are shown in Fig. 22. The gain of the receiver is approximately 20 dB with an RF bandwidth

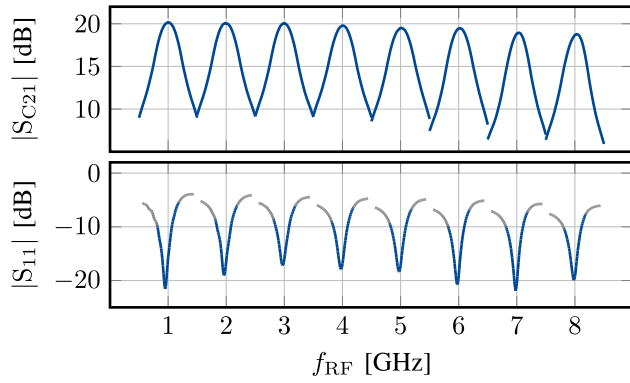


Fig. 22. Measured $|S_{C21}|$ and $|S_{11}|$ for clock frequencies between 1 and 8 GHz.

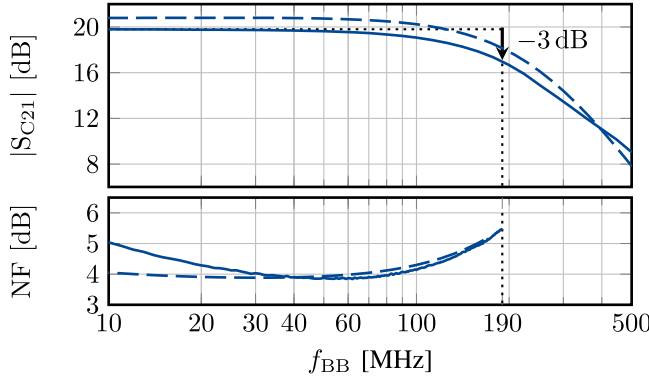


Fig. 23. Measured $|S_{C21}|$ and NF at $f_{LO} = 4$ GHz. Simulation results are added with dashed lines.

of 380 MHz. For the $|S_{11}|$ measurement, we de-embedded the measurement PCB up to the package of the receiver chip. $|S_{11}|$ is better than -10 dB at f_{LO} and around -6 dB at the band edges, caused by the N-path filtering. The notch of $|S_{11}|$ is shifted to slightly lower frequency than f_{LO} due to the bond-wire inductance.

Fig. 23 shows the receiver's gain and NF at $f_{LO} = 4$ GHz along with simulation results (dashed lines). The minimum NF is 3.8 dB and the integrated NF from 10 to 190 MHz is 4.4 dB. The simulated gain and BW are, respectively, 1 dB and 10 MHz larger than measured. The NF is similar. The measured gain at -40 °C is 0.3 dB higher than at room temperature and at 85 °C it is 0.5 dB lower. We measured harmonic rejection at $f_{LO} = 1$ GHz. The HR_3 is 9 dB and HR_5 is 14.1 dB, as expected from a four-phase mixer with 25 % duty-cycle clocks.

We measured the IB IIP₃ of three samples at $f_{LO} = 4$ GHz and at different ambient temperatures to show the robustness of the nonlinearity cancellation in the LNTA over temperature. The result is shown in Fig. 24. Two -25 dBm test tones are applied at the RF input with frequencies $f_1 = f_{LO} + \Delta f - 2$ MHz and $f_2 = f_{LO} + \Delta f + 2$ MHz. The resulting IM₃ tone is measured at $\Delta f - 6$ MHz. We ensured that the IM₃ distortion and noise from the measurement setup is approximately 10 to 20 dB lower than the receiver's IM₃.

The resulting IB IIP₃ is > 14.5 dBm for all samples and temperatures and > 16 dBm at 25 °C. The IB IIP₃ at 25 °C is lowest around the band edge, and seemingly limited by the IIP₃ of the TIA as simulated in Fig. 18. We hypothesize

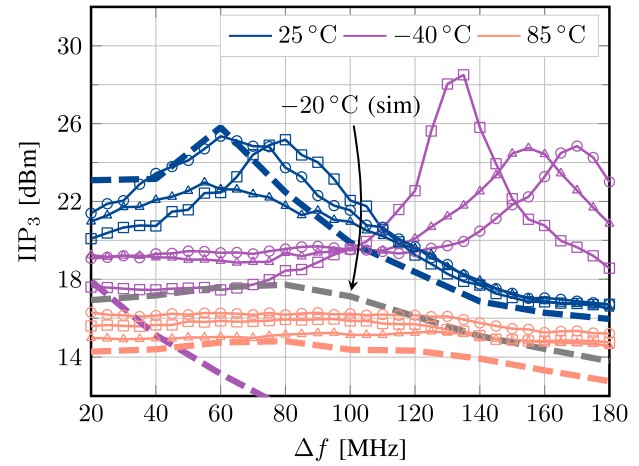


Fig. 24. Measured IB IIP₃ at $f_{LO} = 4$ GHz for three different samples (indicated with markers) and different ambient temperatures. Simulation results are added with dashed lines.

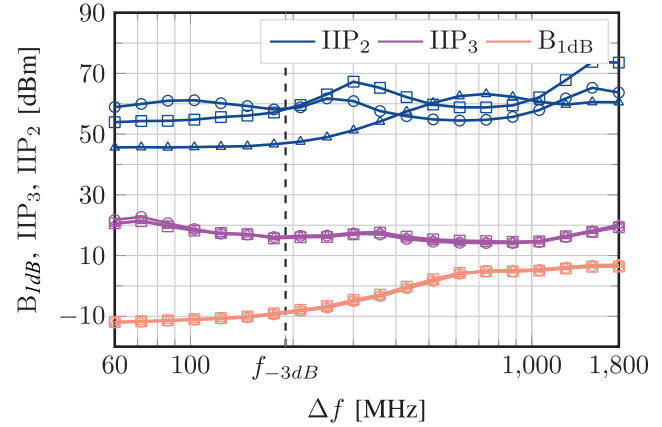


Fig. 25. Measured OOB IIP₂, OOB IIP₃, and blocker compression point at $f_{LO} = 4$ GHz. Three samples are measured and indicated with markers; the results for IIP₃ and B_{1dB} largely overlap.

that the peaks in IIP₃ at -40 °C are due to cancellation of different IM₃ products generated by the N-path switch, LNTA, and TIA. The simulation results are added with dashed lines. The simulations at 25 °C and 85 °C match well with the measurement. However, the simulation at -40 °C has a noticeably lower IIP₃ than the measured value (only 6.5 dBm at f_{-3dB}). We expect that this is due to the tuning range of the LNTA back-gate bias ($V_{B,N1}$) not being large enough in simulation. An additional simulation at -20 °C is added, which matches closer to the measurement. The effect of temperature variation on linearity could be reduced by, e.g., using temperature-dependent nonlinearity cancellation in the LNTA.

In Fig. 25, we show the OOB linearity measurement results for three samples at room temperature. The OOB IIP₃ is measured by applying two -25 dBm test tones at $f_1 = f_{LO} + \Delta f$ and $f_2 = f_{LO} + 2 \cdot \Delta f - 50$ MHz such that $f_{IM3} = 50$ MHz. The resulting OOB IIP₃ is larger than 14 dBm.

It is noted that the IB IIP₃ is better than the OOB IIP₃. This is due to the buffer used in the bootstrap switch. This buffer introduces a phase shift between the residual baseband signal and the bootstrap switch for OOB signals, negating the linearity benefit of the bootstrap switch.

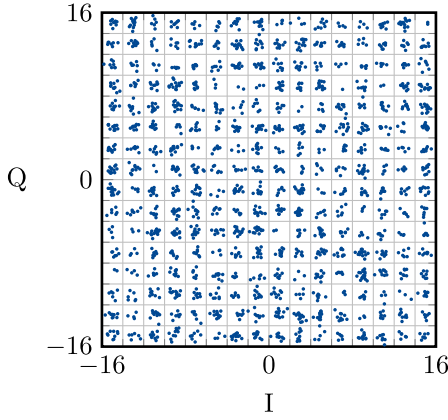


Fig. 26. Measured constellation of a -55 dBm 100 MS/s 256-QAM signal. The corresponding EVM is -30.1 dB.

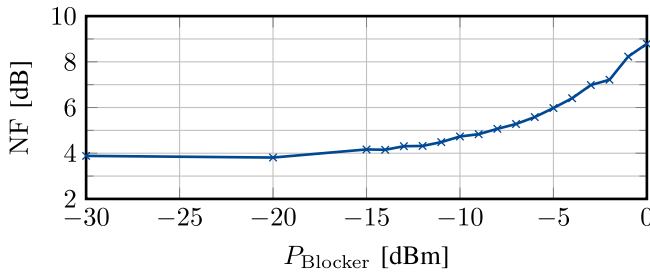


Fig. 27. Measured blocker NF at 50 MHz with $f_{LO} = 4$ GHz and $f_{blocker} = 3.05$ GHz.

The OOB IIP_2 is measured with two -25 dBm test tones at $f_1 = f_{LO} + \Delta f$ and $f_2 = f_{LO} + \Delta f + 50$ MHz, such that $f_{IM2} = 50$ MHz. The resulting IIP_2 is better than 45 dBm. There is a relatively large spread in IIP_2 between the samples, expectedly due to mismatch in the pseudo-differential design.

The blocker compression point is measured by applying a -30 dBm test tone at $f_{LO} + 50$ MHz and a blocker at $f_1 = f_{LO} + \Delta f$. The blocker power at which the test tone is compressed by 1 dB is shown in Fig. 25. For IB frequencies, the compression point is approximately -12 dBm for all samples, limited by the output swing of the TIA. This increases to 6 dBm for OOB frequencies thanks to N-path filtering, which reduces the signal swing at the TIA.

We measured the performance of the receiver when a -55 dBm 100 MS/s 256-QAM signal at 4.1 GHz with $f_{LO} = 4$ GHz is applied. Fig. 26 shows the received constellation. The measured EVM is -30.1 dB. Fig. 27 shows the NF at 50 MHz for $f_{LO} = 4$ GHz when a blocker is applied at $f_{LO} - 5f_{-3dB}$. The 0 dBm blocker NF is 8.8 dB.

Fig. 28 shows the integrated $|S_{C21}|$ and NF across different f_{LO} . The gain and integrated NF degrade 1.4 and 2.2 dB, respectively, from $f_{LO} = 1$ to 8 GHz, showing that the receiver can be used for a wide range of RF input frequencies.

Fig. 29 shows the IB IIP_3 , IIP_2 and B_{1dB} across different f_{LO} . The IB IIP_3 is measured over the entire bandwidth (like in Fig. 24) for three samples at room temperature, where the smallest value within the bandwidth for each sample and f_{LO} is shown in Fig. 29. The IIP_2 is measured at $\Delta f = 60$ MHz and B_{1dB} is measured at $\Delta f = 3f_{-3dB} = 570$ MHz.

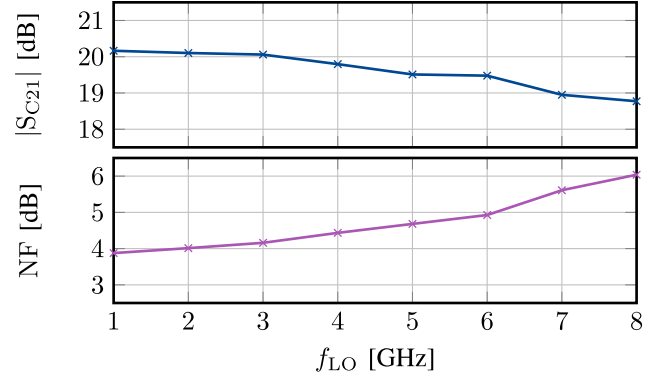


Fig. 28. Measured integrated NF (10–190 MHz) and $|S_{C21}|$ across LO frequencies.

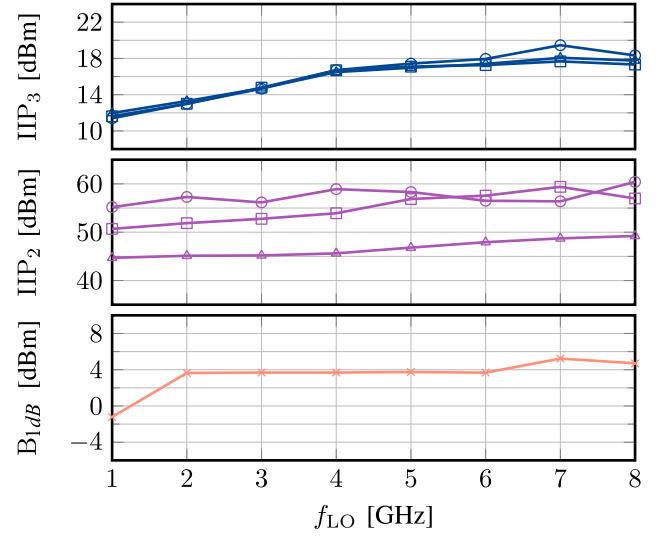


Fig. 29. Measured IB IIP_3 , IIP_2 ($\Delta f = 60$ MHz) and B_{1dB} ($\Delta f = 3f_{-3dB}$) across LO frequencies. For IIP_3 and IIP_2 , three samples are measured and indicated with markers.

The IB IIP_3 does not degrade at high f_{LO} , demonstrating the high speed of the N-path bootstrap switch. For f_{LO} lower than 4 GHz, the IB IIP_3 degrades due to a design error in the voltage buffer employed between the baseband node and the bootstrap switch, as described in Section II-D. An improvement is also given there. The IIP_2 and B_{1dB} do not change much with clock frequency. Only B_{1dB} at $f_{LO} = 1$ GHz is lower as Δf is nearing $2f_{LO}$.

C. Comparison

A comparison with prior-art wideband receivers with over 150 MHz baseband BW is shown in Table II. The reported IIP_3 of our receiver is the minimum measured over the IB/OOB frequencies at $f_{LO} = 4$ GHz. The noise canceling mixer-first receiver by Bhat et al. [3] achieves similar BW and gain but has approximately 7 dB lower IB IIP_3 . It does, however, achieve more broadband input matching and lower NF than our work, at the cost of $> 4\times$ higher power consumption.

The LNTA-based receiver by Jiang et al. [6] achieves a similar IB IIP_3 to our receiver but has a lower gain and higher NF. In addition, our work has approximately $3\times$ lower power consumption.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH WORKS ACHIEVING OVER 150 MHz BB BW

	This Work	Bhat JSSC 2021 [3]	Jiang TCAS-I 2019 [6]	Montazerolghaem JSSC 2025 [7]	Razavi JSSC 2022 [8]
Architecture	Mixer-first	NC Mixer-first	LNTA-based	LNTA-based	LNTA-based
Technology	22 nm FDSOI	22 nm FDSOI	40 nm	40 nm	28 nm
RF Input	Single-Ended	Differential	Differential	Single-Ended	Single-Ended
f_{rf} [GHz]	1 – 8	1 – 6	3 – 6	0.4 – 7.3	0.4 – 6
Gain [dB]	19.8 ^b	22.4	14.5	38	54
BB BW [MHz]	190	175	200	150	160
NF [dB]	4.0 – 6.0 ^a	2.5 – 5.0	5 – 5.8	3.2 – 5.8	4.0 ^f
IB IIP ₃ [dBm]	> 16 ^b	> 9	15.1 – 16.7	–8 – 0 ^d	–35 ^f
IB OIP ₃ [dBm]	> 33 ^b	> 28.5 ^c	28 – 30 ^c	27 – 38	19 ^{ef}
OOB IIP ₃ [dBm]	> 14 ^b	> 12	33	11	3 ^f
B _{1dB} [dBm] ^g	3.7	–1	7.5	–4.8	N/A
EVM [dB]	–30.1 ^h	N/A	N/A	–30.2 ^h	–25.3 ⁱ
Supply Voltage [V]	0.80	0.83	1.8/1.1	1.3	1.0
Active area [mm ²]	0.3	0.48	1.2 ^c	0.42	1.9
Power consumption [mW]	37.6 + 1.1 GHz ^{–1}	162.4 + 1.7 GHz ^{–1}	64.1 – 69.6 ^c	100 + 13 GHz ^{–1}	23 – 49

^a 4.0 – 6.0 is the integrated NF over the BW ^b $f_{LO} = 4$ GHz ^c Only I-channel ^d OIP₃ – Gain ^e IIP₃ + Gain ^f With 160 MHz BW setting
^g $\Delta f/f_{-3dB} \approx 3$ ^h –55 dBm 100 MS/s 256-QAM ⁱ –57 dBm 80 MS/s 256-QAM

The receivers of Montazerolghaem and Babaie [7] and Razavi and Razavi [8] achieve similar NF, but much lower IB IIP₃ than our receiver. They have a higher gain, but our IB OIP₃ is > 6 dB better. Our work has a much lower power consumption and active area. However, these receivers do have better selectivity to suppress OOB signals, although their OOB IIP₃ is not better.

Overall, this work achieves the highest IB IIP₃ with the lowest area and power consumption and with comparable NF compared to state of the art.

VI. CONCLUSION

We propose a receiver with a high 16dBm IB linearity over a 190MHz BB BW, operating over a wide 1–8GHz RF frequency range. We achieve this with a bootstrapped N-path mixer, in which the gate voltage of the mixer switch tracks the receiver's baseband voltage. This mixer switch operates over a large range of LO frequencies. We also present an LNTA that partially cancels its distortion, improving IB IIP₃ without adding significant power consumption. These techniques can be applied to N-path-based receivers to improve linearity at only a minor increase in power consumption.

ACKNOWLEDGMENT

The authors would like to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program. They also thank A. S. Delke for CAD assistance and A. R. Rop for help during measurements.

REFERENCES

- [1] G. Pini, D. Manstretta, and R. Castello, "Analysis and design of a 260-MHz RF bandwidth +22-dBm OOB-IIP₃ mixer-first receiver with third-order current-mode filtering TIA," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1819–1829, Jul. 2020.
- [2] D. H. Mahrof, E. A. M. Klumperink, Z. Ru, M. S. O. Alink, and B. Nauta, "Cancellation of OpAmp virtual ground imperfections by a negative conductance applied to improve RF receiver linearity," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1112–1124, May 2014.
- [3] A. N. Bhat, R. A. R. van der Zee, and B. Nauta, "A baseband-matching-resistor noise-canceling receiver with a three-stage inverter-only OpAmp for high in-band IIP₃ and wide IF applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 1994–2006, Jul. 2021.
- [4] Y.-C. Lien, E. A. M. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1348–1360, May 2018.
- [5] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
- [6] J. Jiang, J. Kim, A. I. Karsilayan, and J. Silva-Martinez, "A 3–6-GHz highly linear I-channel receiver with over +3.0-dBm in-band P1dB and 200-MHz baseband bandwidth suitable for 5G wireless and cognitive radio applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3134–3147, Aug. 2019.
- [7] M. A. Montazerolghaem and M. Babaie, "A sub-7-GHz linear receiver for 5G local area base station applications," *IEEE J. Solid-State Circuits*, early access, Mar. 27, 2025, doi: 10.1109/JSSC.2025.3551673.
- [8] H. Razavi and B. Razavi, "A 0.4–6 GHz receiver for cellular and WiFi applications," *IEEE J. Solid-State Circuits*, vol. 57, no. 9, pp. 2640–2657, Sep. 2022.
- [9] S. Krishnamurthy, L. Iotti, and A. M. Niknejad, "Design of high-linearity mixer-first receivers for mm-wave digital MIMO arrays," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3375–3387, Nov. 2021.
- [10] E. A. Klumperink, H. J. Westerveld, and B. Nauta, "N-path filters and mixer-first receivers: A review," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Feb. 2017, pp. 1–8.
- [11] F. Tillman and H. Sjolund, "A bootstrapping technique to improve the linearity of CMOS passive mixers," in *Symp. VLSI Circuits. Dig. Tech. Papers*, 2003, pp. 221–222.
- [12] A. Nagulu, Y. Zhuang, M. Yuan, S. Garikapati, and H. Krishnaswamy, "A third-order quasi-elliptic N-path filter with enhanced linearity through clock boosting," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3351–3363, Dec. 2023.
- [13] R. Chen and H. Hashemi, "Passive coupled-switched-capacitor-resonator-based reconfigurable RF front-end filters and duplexers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 138–141.
- [14] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, "An 8 bit 4 GS/s 120 mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.
- [15] M. Baraani Dastjerdi, S. Jain, N. Reiskarimian, A. Natarajan, and H. Krishnaswamy, "Analysis and design of a full-duplex two-element MIMO circulator-receiver with high TX power handling exploiting MIMO RF and shared-delay baseband self-interference cancellation," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3525–3540, Dec. 2019.
- [16] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

- [17] Y. Nakagome et al., "An experimental 1.5-V 64-mb DRAM," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 465–472, Apr. 1991.
- [18] B. J. Thijssen, E. A. M. Klumperink, P. Quinlan, and B. Nauta, "2.4-GHz highly selective IoT receiver front end with power optimized LNTA, frequency divider, and baseband analog FIR filter," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2007–2017, Jul. 2021.
- [19] H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 22–36, Jan. 2011.
- [20] H. Kundur Subramaniam, E. A. M. Klumperink, V. Srinivasan, A. Kiaei, and B. Nauta, "RF transconductor linearization robust to process, voltage and temperature variations," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2591–2602, Nov. 2015.



Erwin Hardeveld (Graduate Student Member, IEEE) was born in Bilthoven, The Netherlands. He received the M.Sc. degree in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2018, where he is currently pursuing the Ph.D. degree with the Integrated Circuits Design Group.

His current research interests include receiver front ends and clock generation circuits.



Ronan van der Zee (Member, IEEE) received the M.Sc. degree (cum laude) in electrical engineering and the Ph.D. degree in high-efficiency audio power amplifiers from the University of Twente, Enschede, The Netherlands, in 1994 and 1999, respectively.

In 1999, he joined Philips Semiconductors, Eindhoven, where he worked on class AB and class D audio power amplifiers. In 2003, he joined the IC-Design Group, University of Twente, where his research has developed in the directions of both RF front ends and switched-mode power amplifiers.

Dr. Zee has served as a Technical Program Committee (TPC) Member for European Solid State Circuit Conference (ESSCIRC, now ESSERC). He was a co-recipient of the ISSCC 2025 "Van Vessel Outstanding Paper Award." He was a Guest Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC).



Bram Nauta (Fellow, IEEE) was born in Hengelo, The Netherlands. He received the M.Sc. degree (cum laude) in electrical engineering and the Ph.D. degree in analog CMOS filters for very high frequencies from the University of Twente, Enschede, The Netherlands, in 1987 and 1991, respectively.

In 1991, he joined the Mixed-Signal Circuits and Systems Department, Philips Research, Eindhoven. In 1998, he returned to the University of Twente as a Full Professor, heading the new IC Design Group.

In 2014, he was nominated as a Distinguished Professor, and from 2016 to 2020, he was the Chair of the Electrical Engineering Department. In 2022, he co-founded "ChipTechTwente," a local ecosystem initiative with 50 semiconductor-related companies, partners, and knowledge institutions. His research interests include analog and radio frequency CMOS circuits.

Dr. Nauta is a member of the Royal Netherlands Academy of Arts and Sciences (KNAW). He was a co-recipient of the ISSCC 2002 and 2009 "Van Vessel Outstanding Paper Award." In 2023, he received the ISSCC Author-Recognition Award for its first 70 years as a top ten contributor. In 2014, he received the "Simon Stevin Meester" Award (500 000 Euros), the Largest National Prize in The Netherlands for achievements in engineering sciences. In 2019, he received an European Research Council (ERC) Advanced Grant (2.5 Million Euros, personal grant). In 2023, he received the inaugural "Dutch Innovation Award" and the NWO Stevin Prize (1.5 Million Euros), the largest national science prize in The Netherlands for "Exceptional Success in Knowledge Exchange and Impact for Society." He was the 2013 Program Chair of the International Solid-State Circuits Conference (ISSCC). He served as the Editor-in-Chief for IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) from 2007 to 2010. Also, he served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 1997 to 1999 and IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2001 to 2006. He was on the Technical Program Committee of the Symposium on VLSI Circuits from 2009 to 2013 and served on the Steering Committee and Program Committee of European Solid-State Circuit Conference (ESSCIRC) from 1999 to 2017. He served on the Program Committee from 2003 to 2013 and the Executive Committee of ISSCC from 2007 to 2015 and since 2022. In 2023, he joined the Program Committee of the Advances in Analog Circuit Design Workshop Series (AACD). He was the President of the IEEE Solid-State Circuits Society from 2018 to 2019. He served two terms as a Distinguished Lecturer for the IEEE Solid-State Circuits Society.